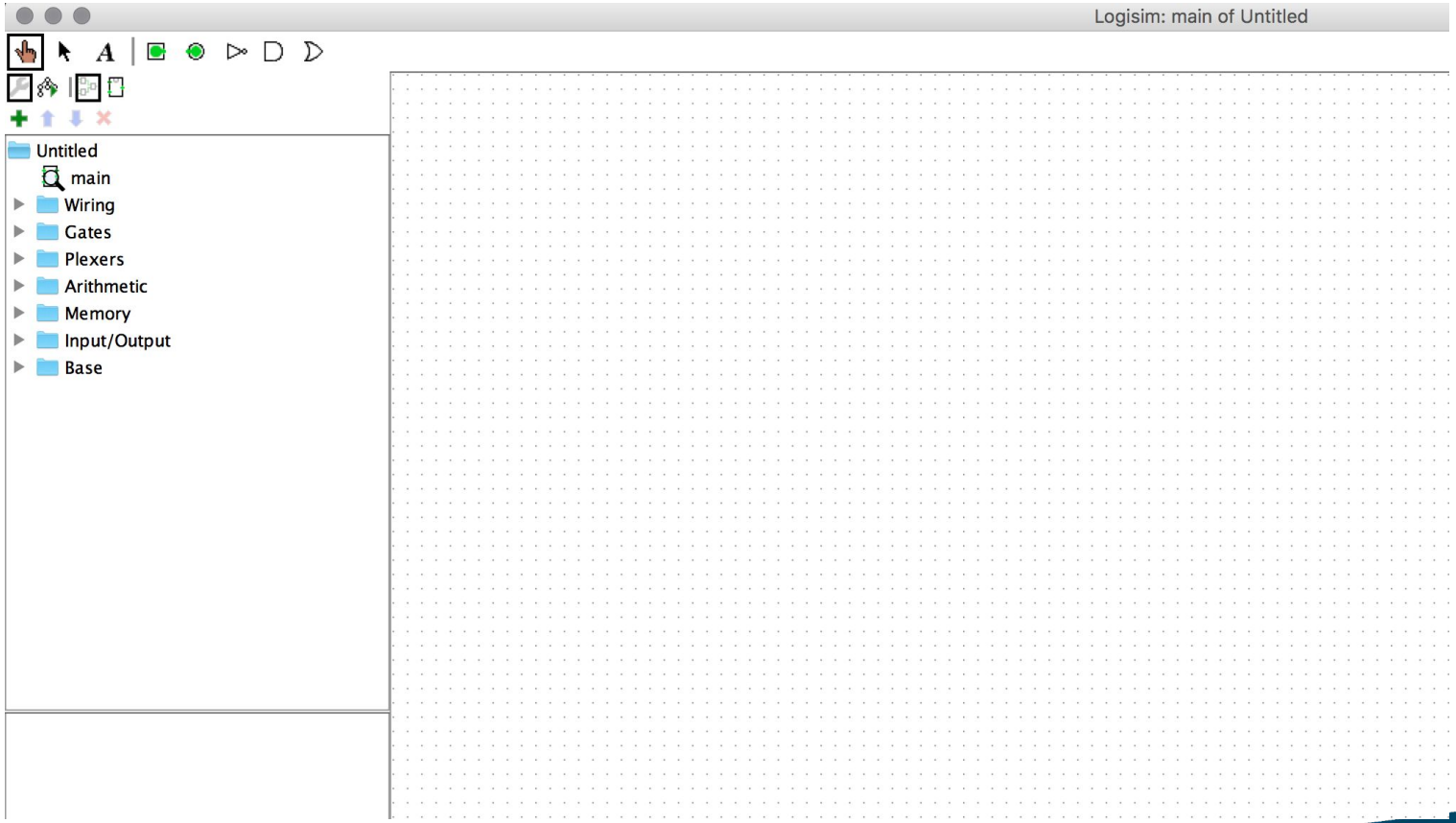
Computer Architecture: Gates and Wires

Brent van Bladel

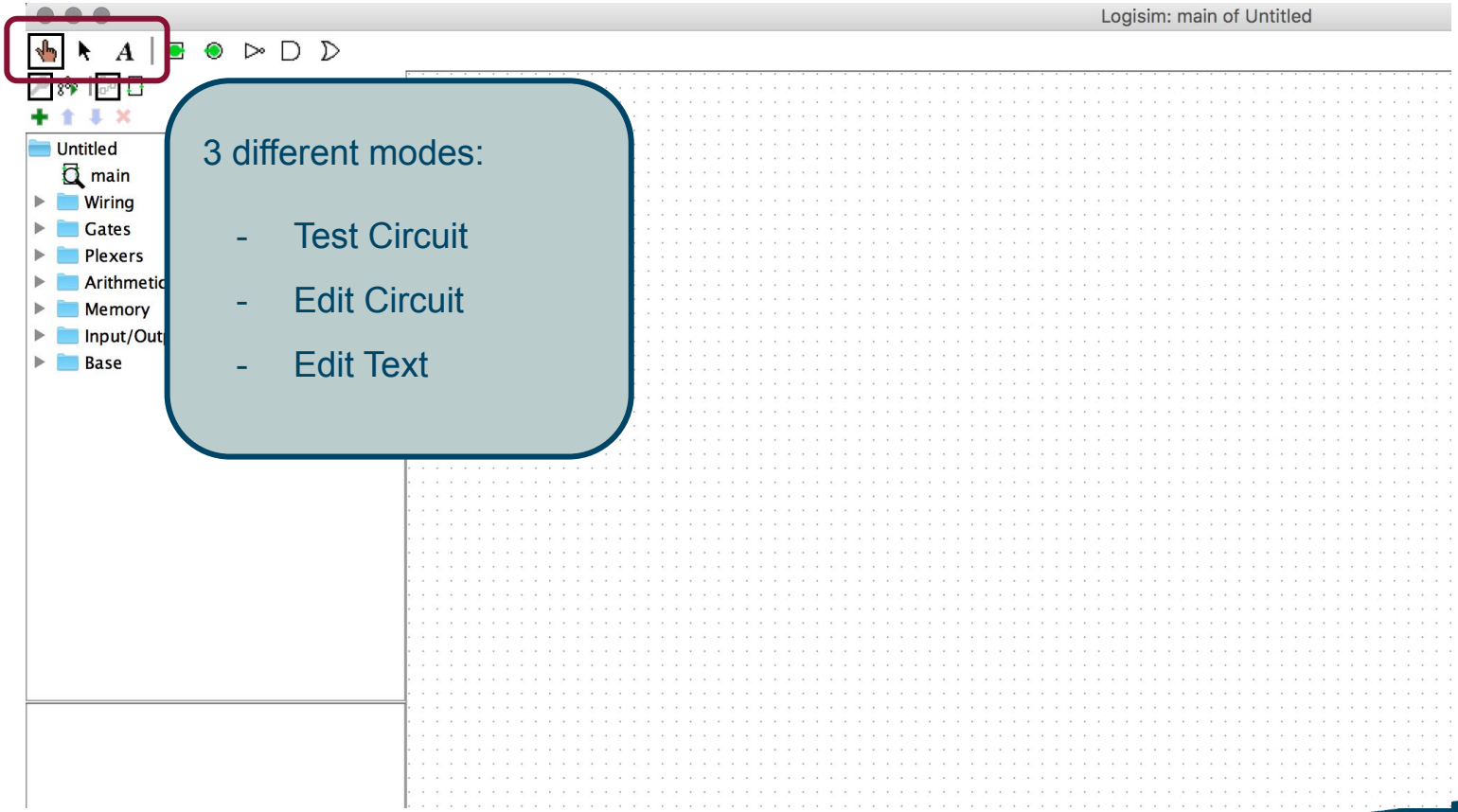
Stephen Pauwels

Universiteit Antwerpen

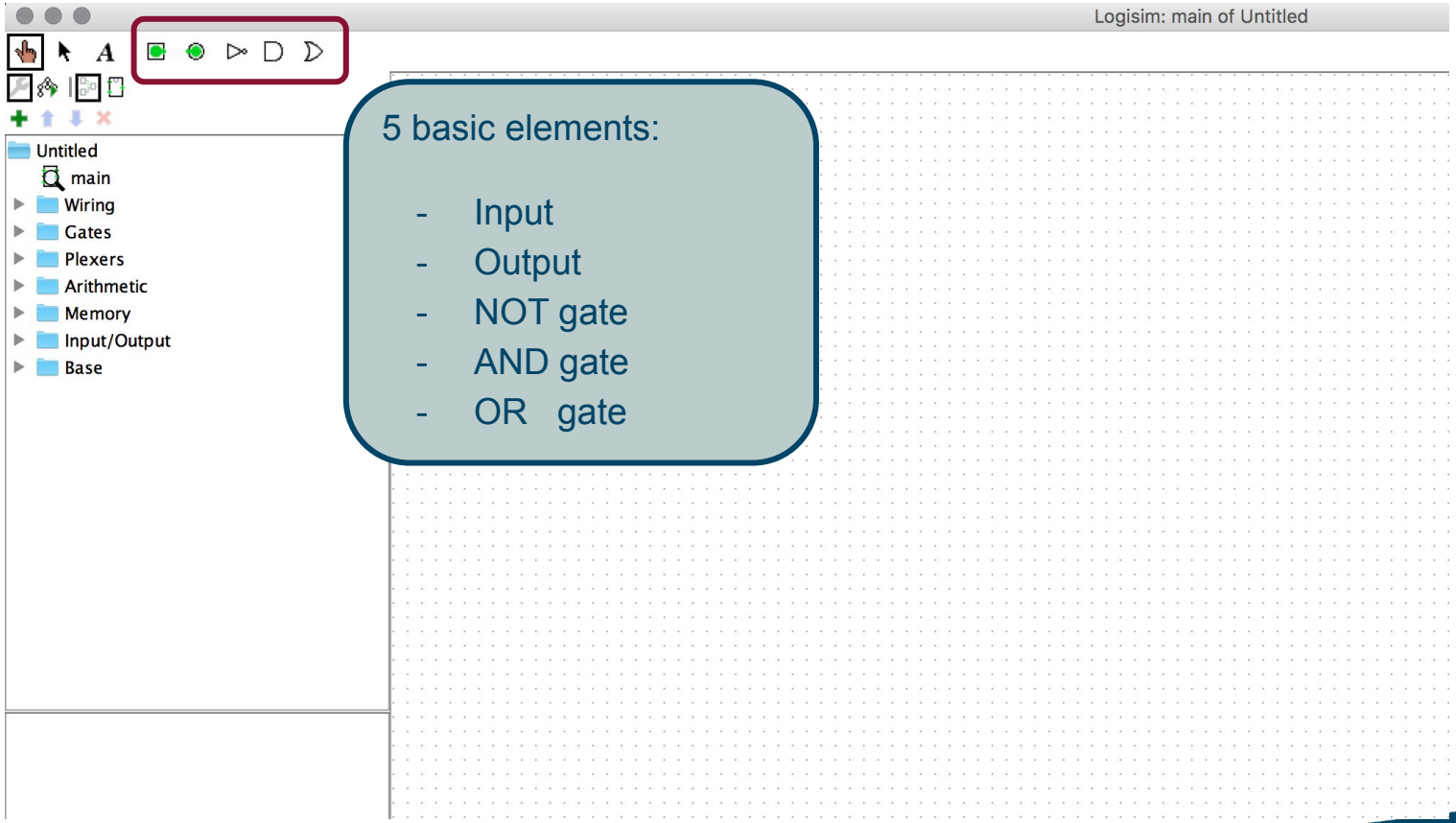
Logisim


Logisim: main of Untitled
Untitled
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base

Logisim


Logisim: main of Untitled
Untitled
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Out
Base
3 different modes:
- Test Circuit
- Edit Circuit
- Edit Text

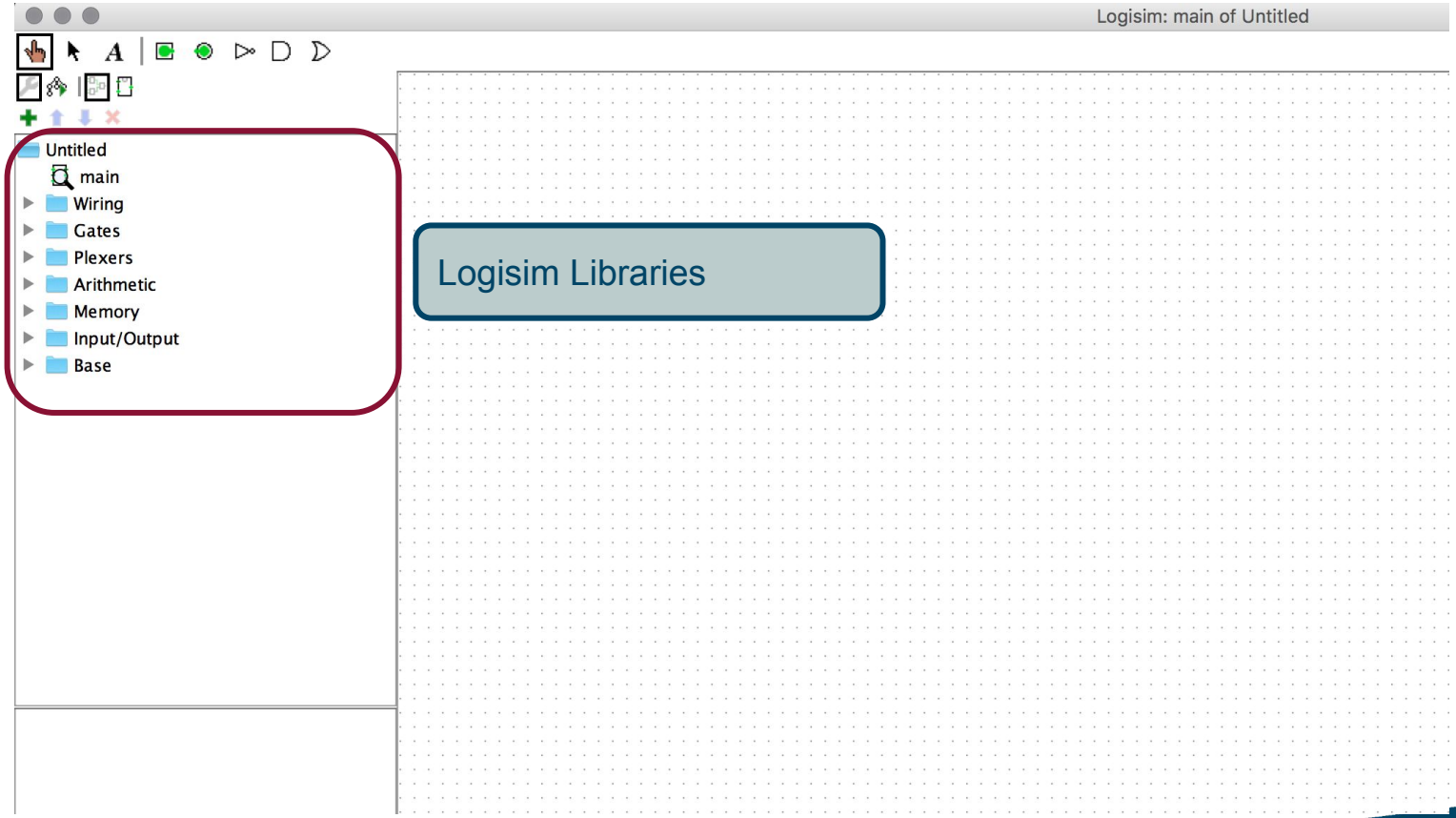
Logisim

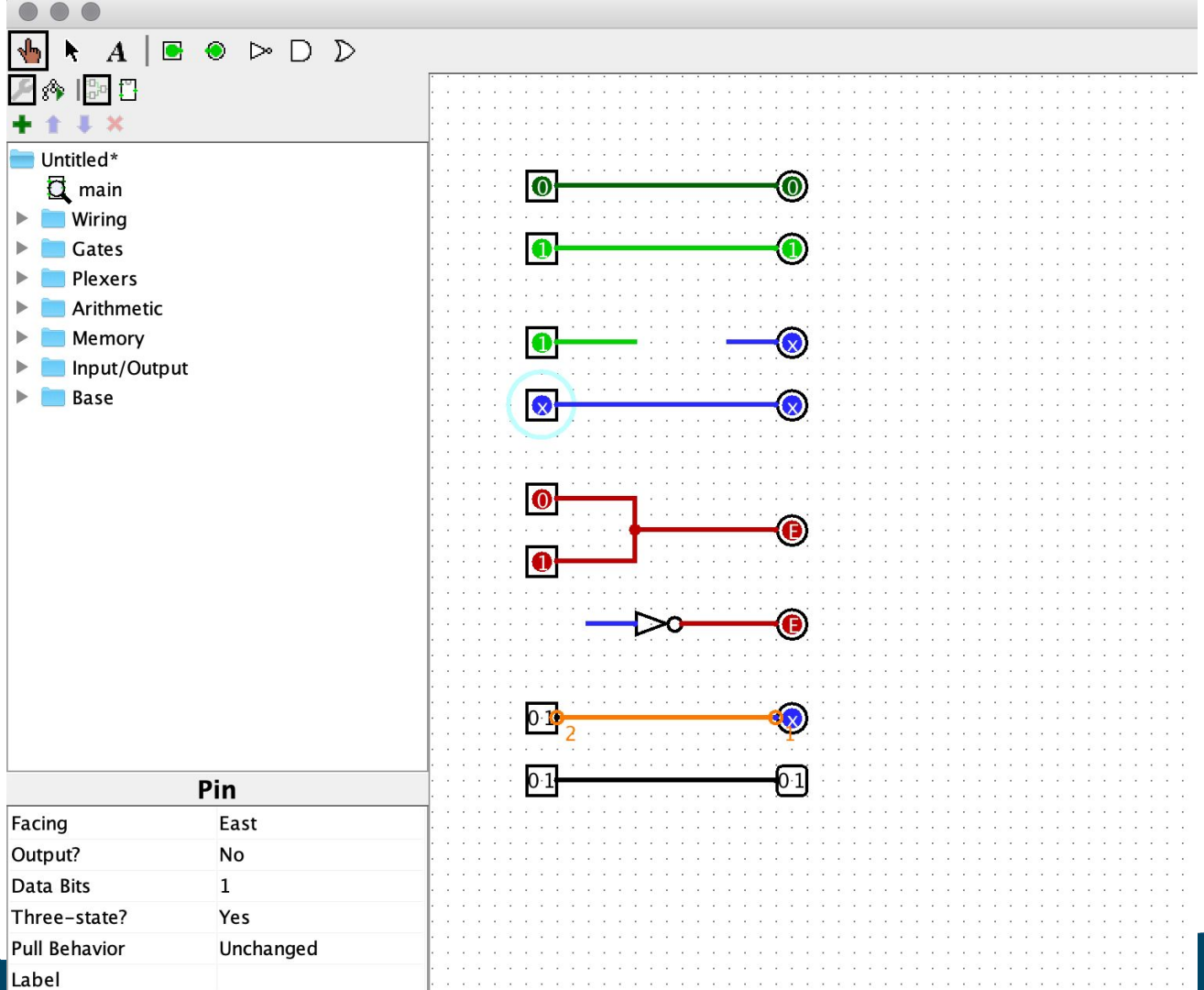


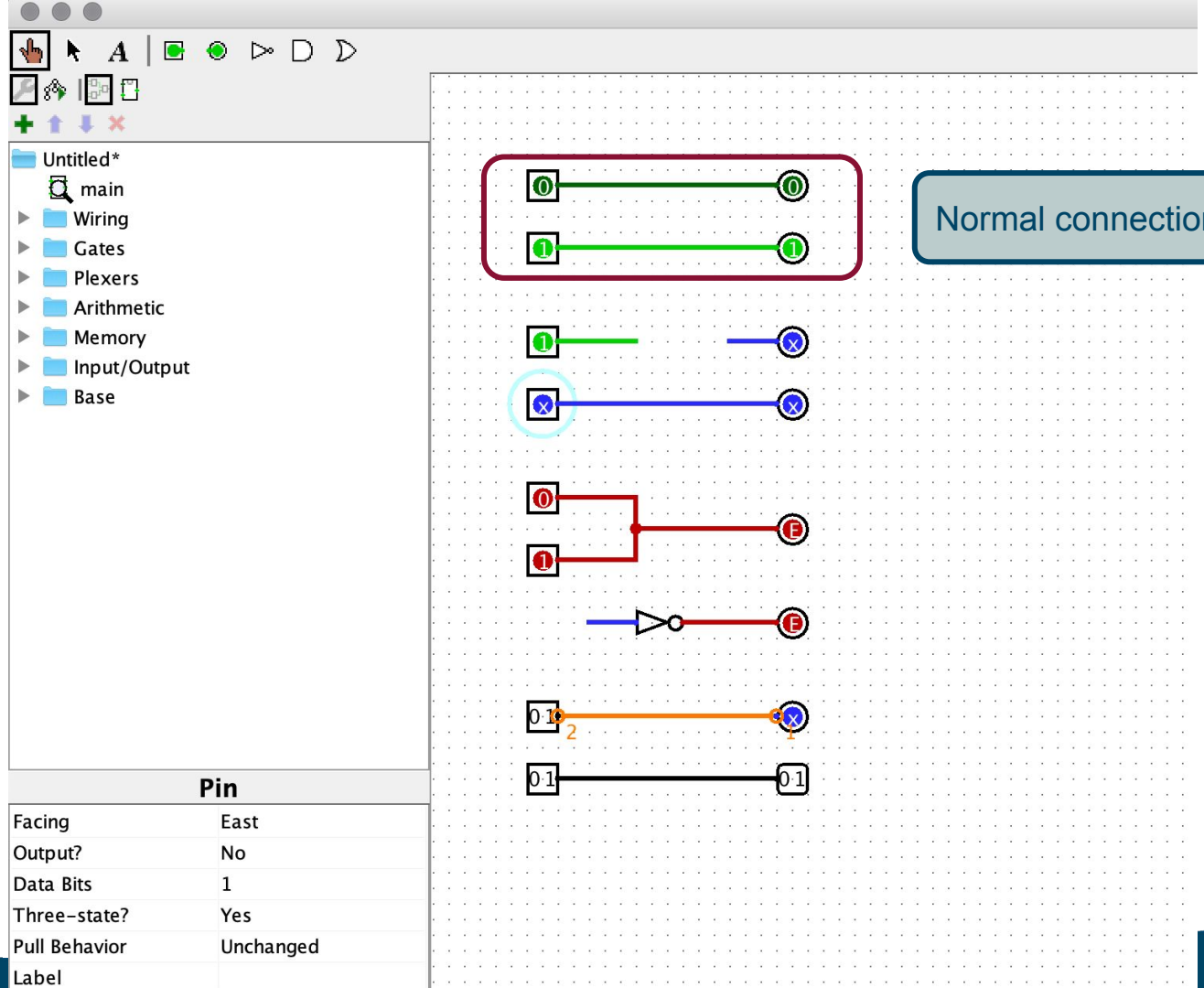
5 basic elements:

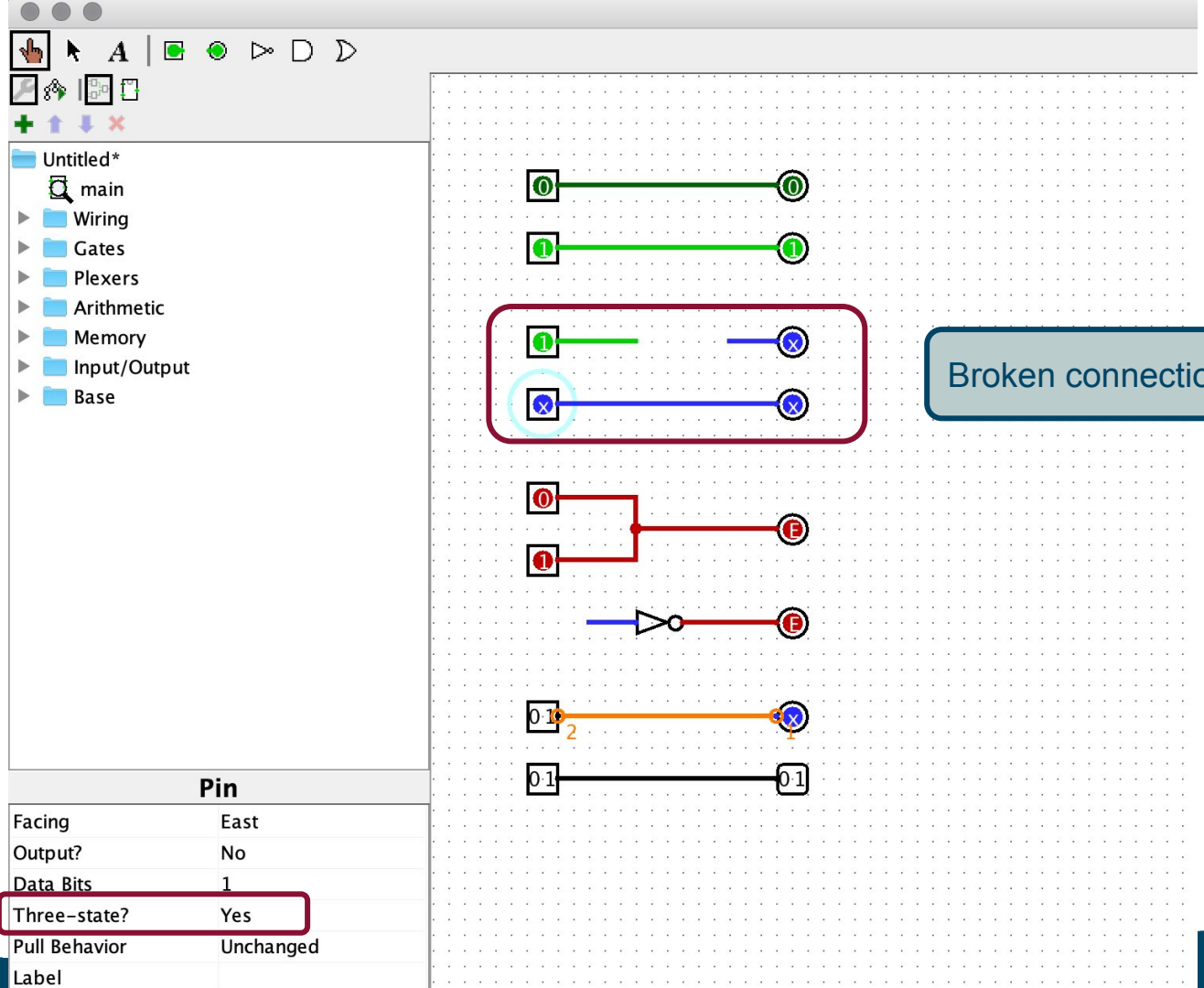
- Input
- Output
- NOT gate
- AND gate
- OR gate

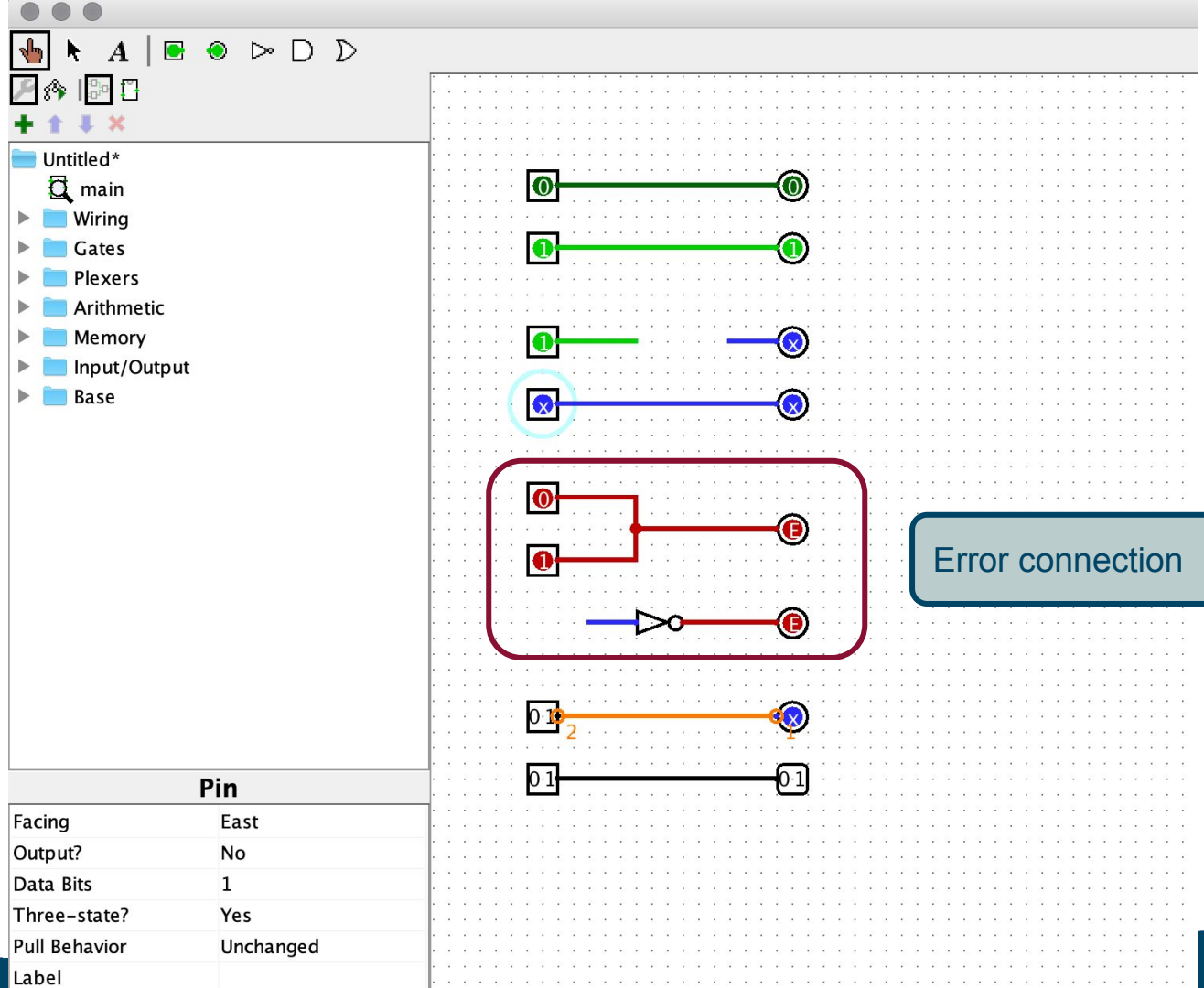
Logisim

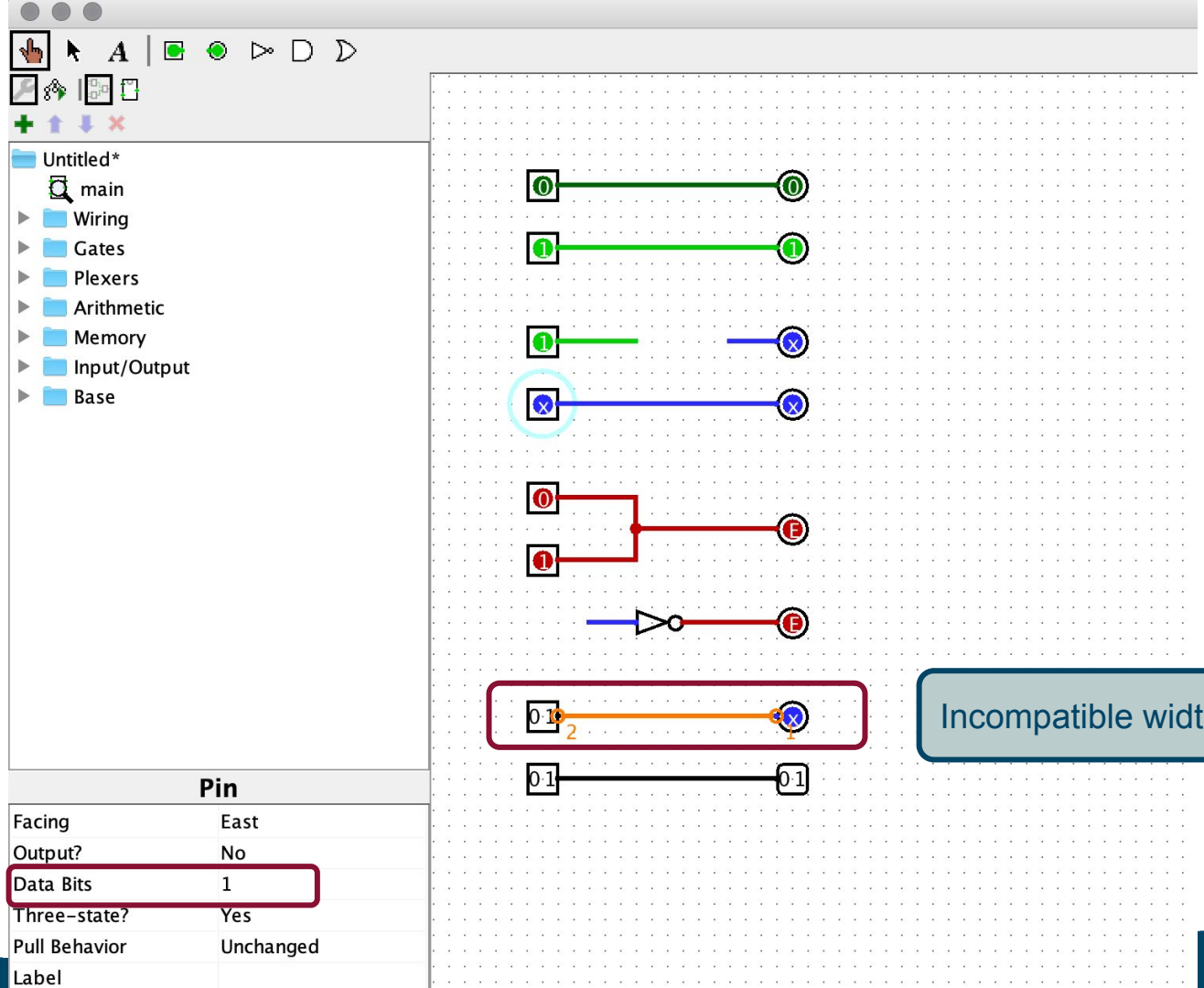

Logisim: main of Untitled
Untitled
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Logisim Libraries

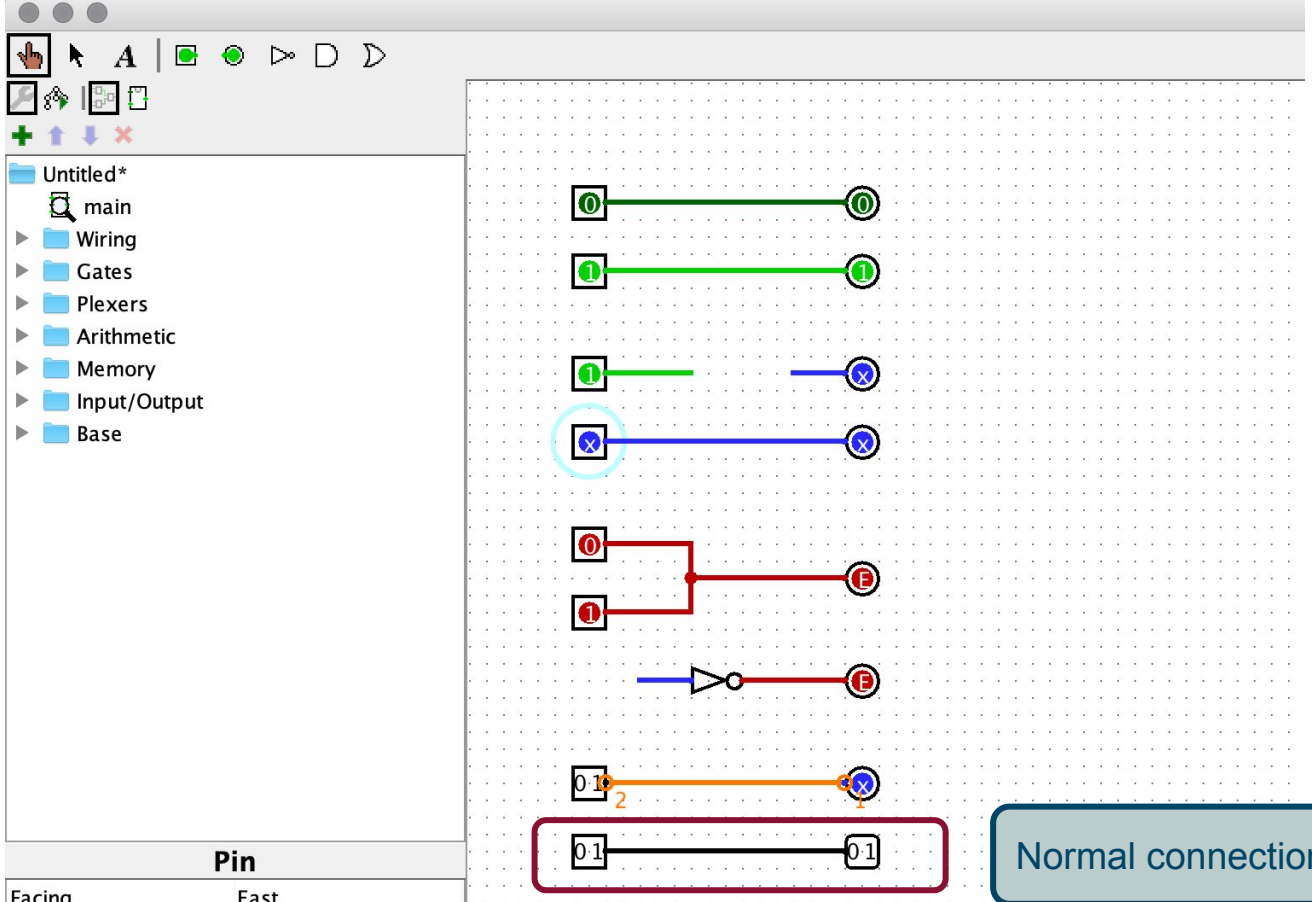

Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label


Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label
Normal connection: 0 or 1

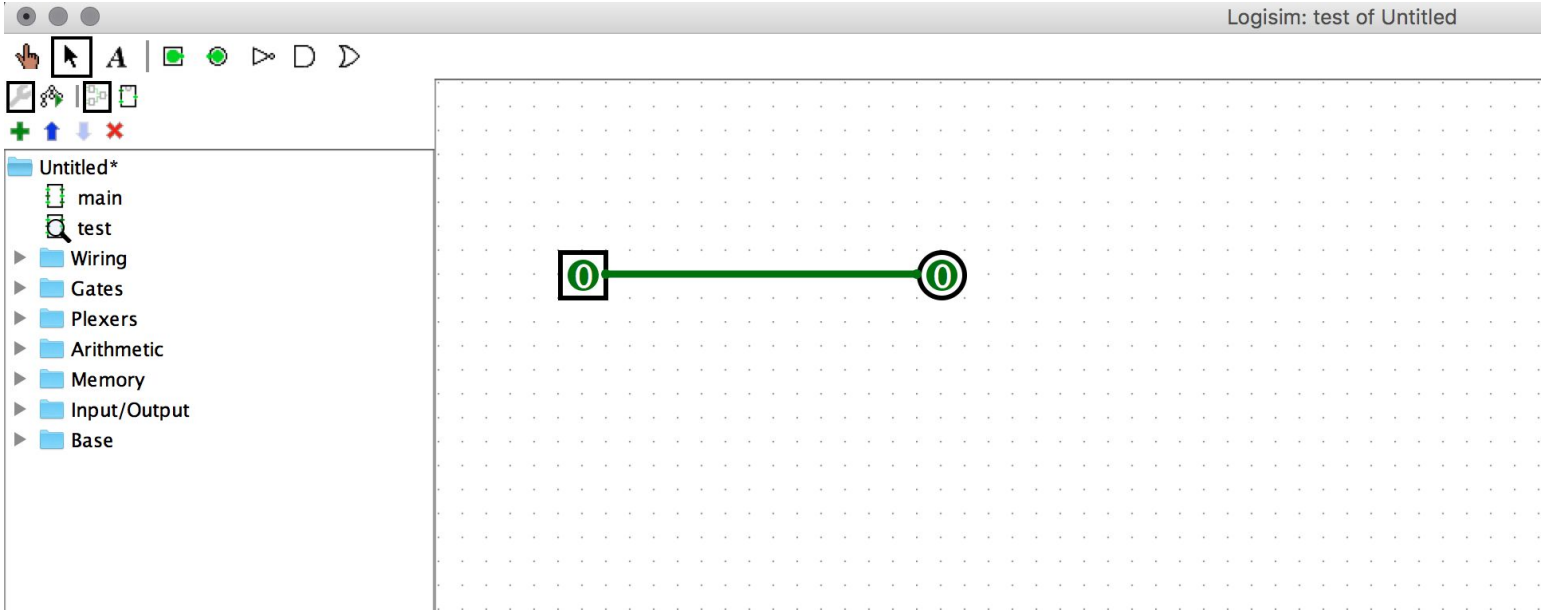

Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label
Broken connection


Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label
Error connection

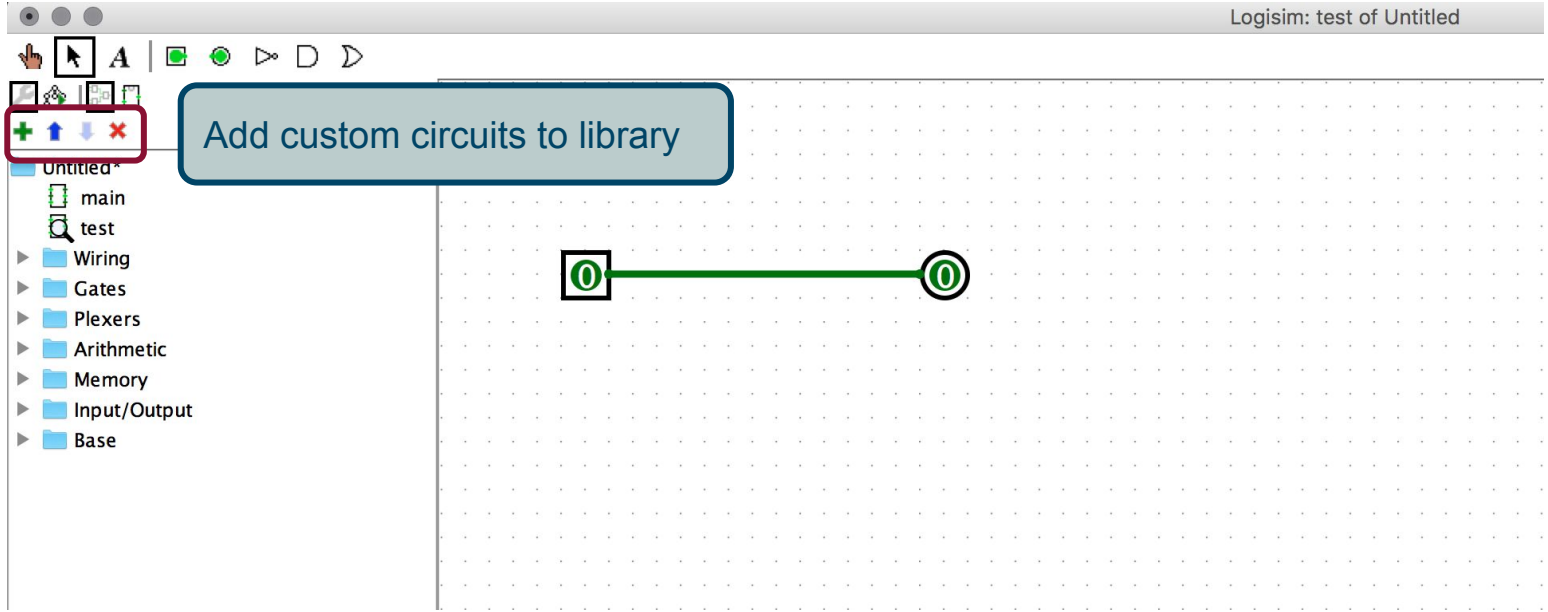

Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label
0
1
x
E
0 1
2
1
Incompatible width


Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? Yes
Pull Behavior Unchanged
Label
0
1
x
E
0-1
2
1
Normal connection: 2 bit

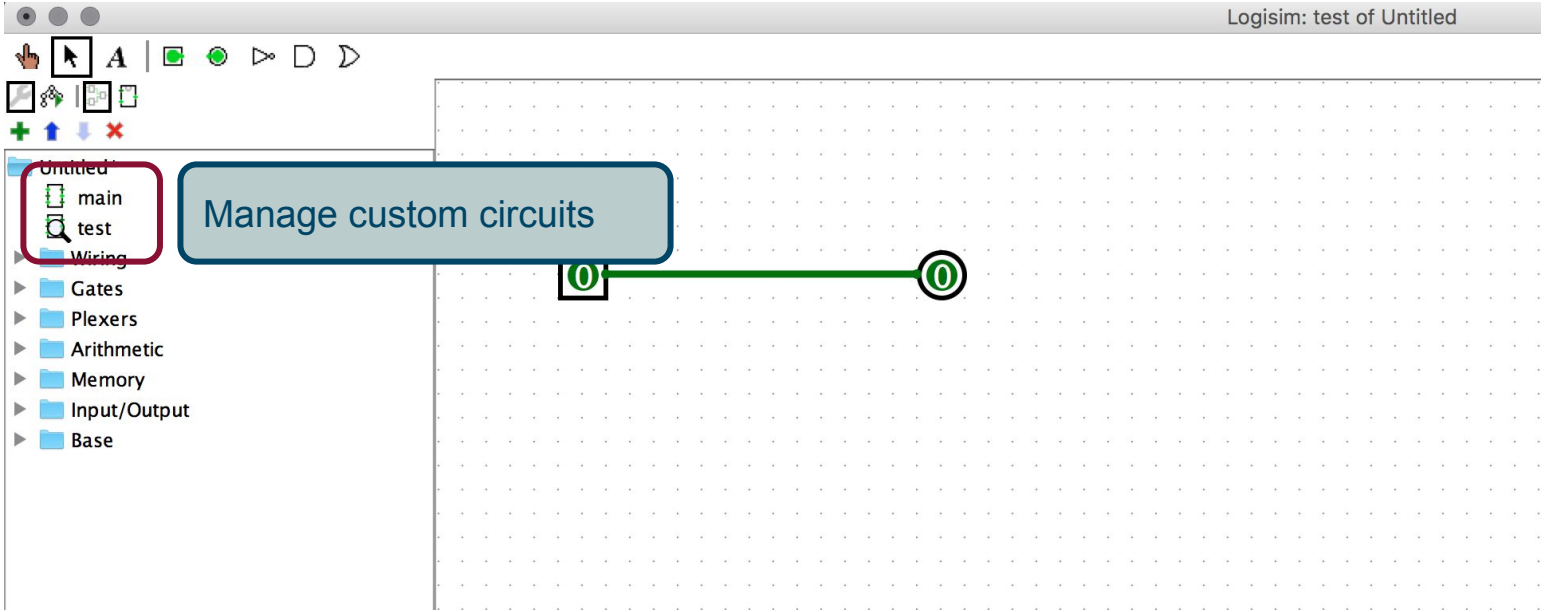
Logisim


Logisim: test of Untitled
Untitled*
main
test
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
0
0

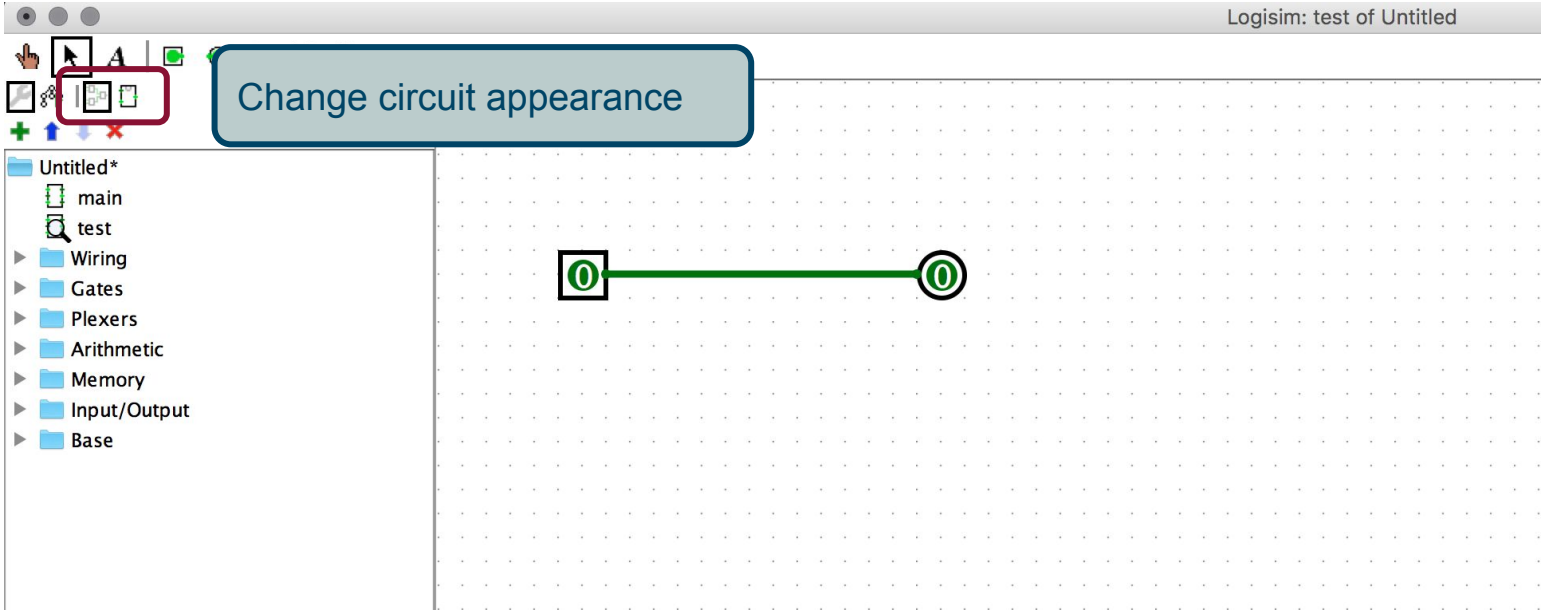
Logisim


Logisim: test of Untitled
Add custom circuits to library
Untitled*
main
test
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
0
0

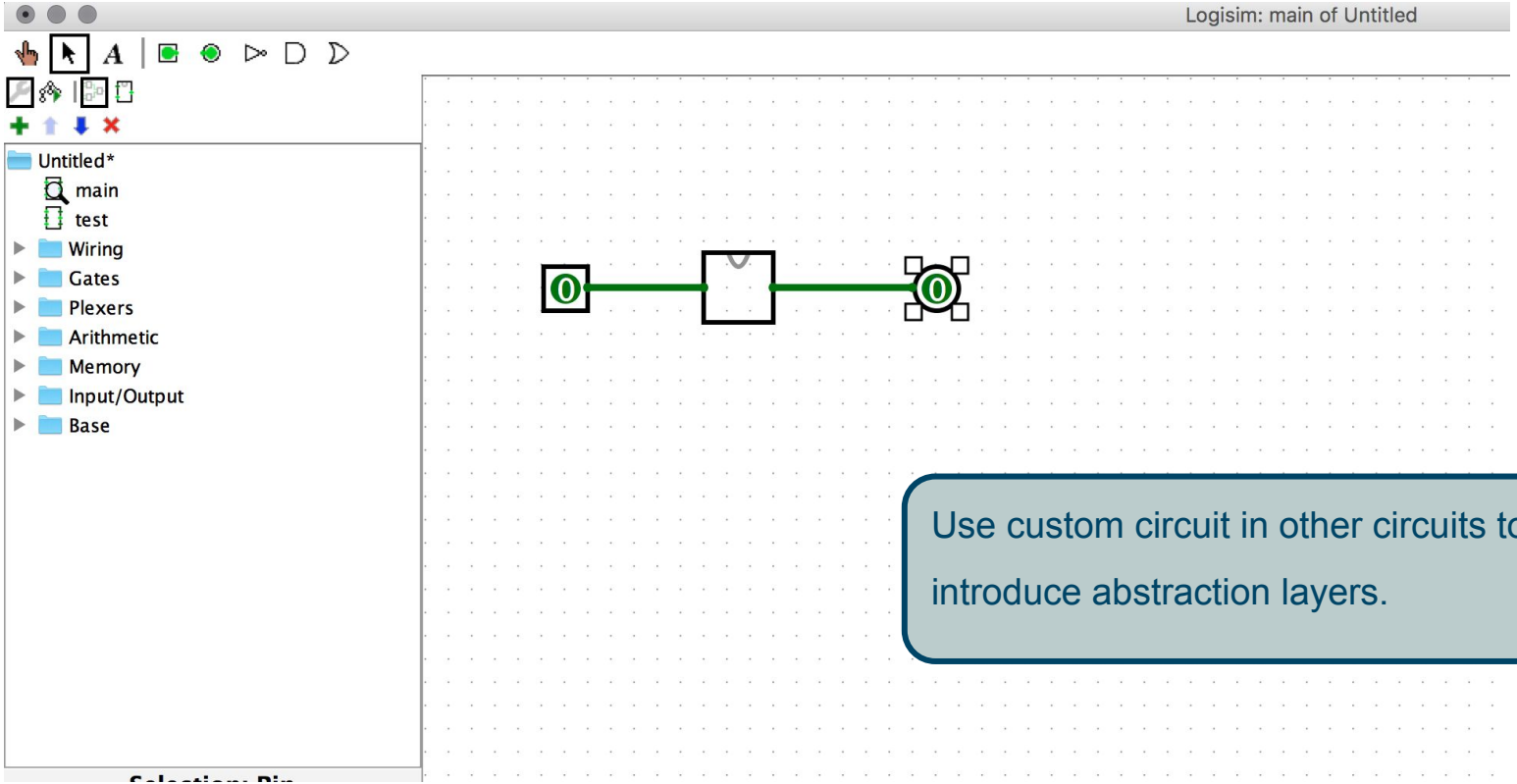
Logisim


Logisim: test of Untitled
Untitled
main
test
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Manage custom circuits
0
0

Logisim


Logisim: test of Untitled
Change circuit appearance
Untitled*
main
test
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
0
0

Logisim



Use custom circuit in other circuits to introduce abstraction layers.

Computer Systems and Architecture

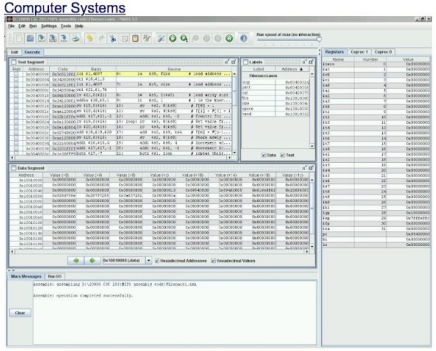
On this page you will find information about the course "Computersystemen en -architectuur" (1001WETCAR) for the first semester of the 2018-2019 academic year at the University of Antwerp.

This page is under construction! You will still find some of last year's material (such as assignments).

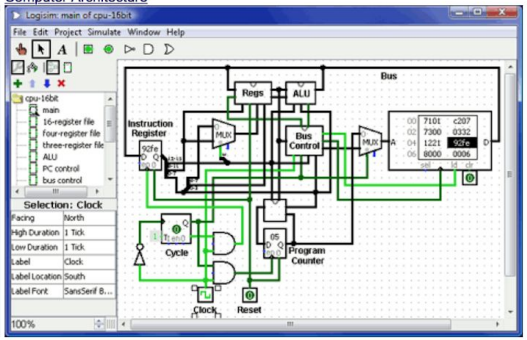
This page is written in English for the benefit of foreign Erasmus students. Note that the course is taught in Dutch however!

This course consists of two interwoven parts:

Computer Systems



Computer Architecture



For which parts of the book correspond to the lectures, have a look at the overview of what to study for the exam.

Exams

First Session

Your total score for this course is calculated as follows:

- During the semester: permanent evaluation counts for 55% of the course grade.
  - Permanent evaluation: Assignments Computer Systems
  - Permanent evaluation: Projects Computer Architecture

  Assignments and Projects are handed in via Blackboard. Projects are evaluated during an oral defense.
- Examination period: the Theory exam counts for 25% of the course grade.
  The course material covered by the theory exam is described in this overview of what to study for the exam.
- Examination period: the practical exam together with its oral defense counts for 20% of the course grade.
  - Examination period: Practical exam (in computer lab: preparation of the design of a datapath as well as translating a high-level program to that architecture)
  - Examination period: Defense of practical exam with questions to test Computer Systems background
- To pass the course, you need to attend or submit *every part* that will be graded (if not, your grade will be "AFW" - absent). Additionally, you need to get an overall score of at least 50%, *and* a score of at least 40% on the theory exam, *and* a score of at least 40% on the practical exam, *and* a score of at least 40% on the year projects (architecture and systems combined). If not, your grade will be `min(7, your_score)`. `your_score` is the score you would get when applying the weights given above.

Second Session

- The weights of the different parts of the course remain the same as during the January session:
  - 25% theory-exam
  - 20% practical-exam

Planning

Week	Date	Time	Type	Room	Computer Systems	Computer Architecture
1	Friday 1 October 2021	8:30 - 12:45	Theory	M.A.143	Course Introduction + Practical Information	From Analog to Digital Logic Design, Logic Gates
2	Tuesday 5 October 2021	10:45 - 12:45	Theory	**G.T.148**	Computer Abstraction	
2	Wednesday 6 October 2021	10:45 - 12:45	Theory	M.A.143	Performance (model)	
2	Thursday 7 October 2021	10:45 - 12:45	Theory	M.A.143	Performance (empirical)	ALU, Adders
2	Friday 8 October 2021	13:45 - 18:00	Lab session	M.G.025 (Group A) M.G.026 (Group B)	Introduction to UNIX	Gates and Wires
3	Tuesday 12 October 2021	10:45 - 12:45	Theory	**G.T.148**		ALU, Adders
3	Wednesday 13 October 2021	10:45 - 12:45	Theory	M.A.143	Data Representation (unsigned integers)	
3	Thursday 14 October 2021	10:45 - 12:45	Theory	M.A.143	Data Representation (signed integers, fixed point)	
3	Friday 15 October 2021	13:45 - 18:00	Lab session	M.G.025 (Group A) M.G.026 (Group B)	Regular Expressions	Adders
4	Wednesday 20 October 2021	10:45 - 12:45	Theory	M.A.143	Data Representation ((IEEE-754) Floating Point)	
4	Thursday 21 October 2021	10:45 - 12:45	Theory	M.A.143	Data Representation (ASCII/EBCDIC)	
4	Friday 22 October 2021	13:45 - 18:00	Lab session	M.G.025 (Group A) M.G.026 (Group B)	UNIX Scripting	ALU
5	Wednesday 27 October 2021	10:45 - 12:45	Theory	M.A.143	Data Representation (Unicode character representations)	
5	Thursday 28 October 2021	10:45 - 12:45	Theory	M.A.143		Memory
5	Friday 29 October 2021	13:45 - 18:00	Lab session	M.G.025 (Group A) M.G.026 (Group B)	vi	Continue work on ALU
5	Sunday 31 October 2021	23:55	Project deadline	Blackboard		Project 1 - 3: Gates and Wires, Adders, ALU
6	Wednesday 3 November 2021	10:45 - 12:45	Theory	M.A.143		Finite State Machines
6	Thursday 4 November 2021	10:45 - 12:45	Theory	M.A.143		Simple Datapath
6	Friday 5 November 2021	13:45 - 18:00	Lab session	M.G.025	Data Representatie	
6	Friday 5 November 2021	13:45 - 18:00	Evaluation and Feedback	M.G.026		Evaluation