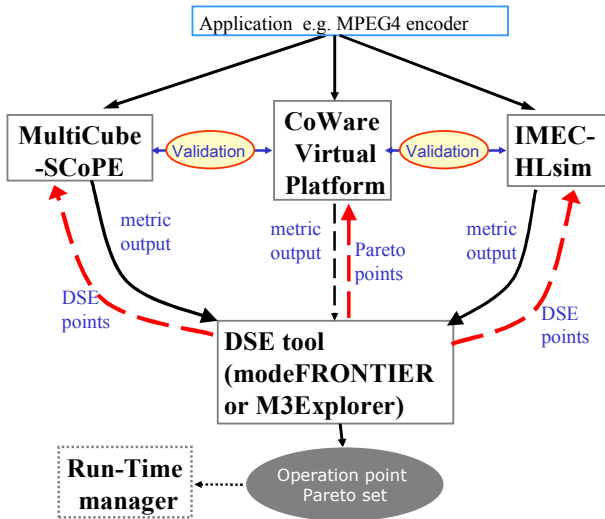


High-level simulators used in EU-MULTICUBE project, enable a multi-abstraction-level system specification and modeling framework to provide **static and dynamic evaluation** of the **system-level performance metrics** (e.g. execution time, energy consumption). These simulators are coupled with Design-Space Exploration (DSE) tools (using a common XML interface) to generate **Pareto set of optimum system configurations** for a specified application on a specified platform. This Pareto set (of optimum configurations) is used by a **Run-Time Manager** during the application run to optimize platform resource usage.



Motivation for various abstraction levels of simulation :

- DSE for an application running on a specific platform requires a large number of application runs (typically on platform simulator).
- There is a trade-off between the accuracy of the simulation results and the time taken for simulating the application.
- Using multiple simulators at various abstraction levels enables DSE to be done with faster higher-level simulators (e.g. IMEC-HLsim and MultiCube-SCoPE). The DSE end results (Pareto set of optimum points) are verified using more accurate platform simulator (i.e. cycle-accurate simulator e.g. CoWare Virtual Platform).
- To maintain interoperability of the application code across various abstraction levels, a **Run-Time Library (RTLlib)** API is defined to specify platform-dependent part of the application e.g. thread spawning, communication, synchronization. Each abstraction level simulator links its own implementation of RTLlib with the application.

MultiCube-SCoPE simulator [1]:

XML description	<ul style="list-style-type: none"> ✓ Support for TLM SystemC components ✓ RTOS models ✓ Native execution of annotated SW code ✓ Dynamic/static SW estimation and annotation 	Performance estimation e.g. energy consumption, exec time
SW code		
App-specific HW models		

MultiCube-SCoPE

IMEC-HLsim simulator [2]:

Platform architecture description	<ul style="list-style-type: none"> ✓ Thread and timing-aware execution ✓ Platform-dependent models for thread communication, synchronization ✓ Models for HW resources e.g. DMA ✓ Timing estimation on compiler-optimized code 	Performance estimation e.g. energy consumption, exec time
SW code		
Execution cycle counts from ISS		VCD trace of app run

IMEC-HLsim

CoWare virtual platform :

- ✓ SystemC based, instruction and cycle accurate, TLM models of the platform resources
- ✓ Detailed Analysis of the resource usage e.g. bus accesses

Design Space Exploration (DSE) :

Hooking up the simulators with DSE tools to generate Pareto set of platform configurations.

References:

- 1) J. Castillo, V. Fernández, H. Posadas, D. Quijano, E. Villar: "SystemC Platform Modeling for Behavioral Simulation and Performance Estimation of Embedded Systems", in the book "Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation". IGI International ed (to be published).
- 2) R. Baert, E. Brockmeyer, S. Wuytack, T. J. Ashby, "Exploring Parallelizations of Application for MPSoC platforms using MPA", Design, Automation and Test in Europe (DATE), 2009 .