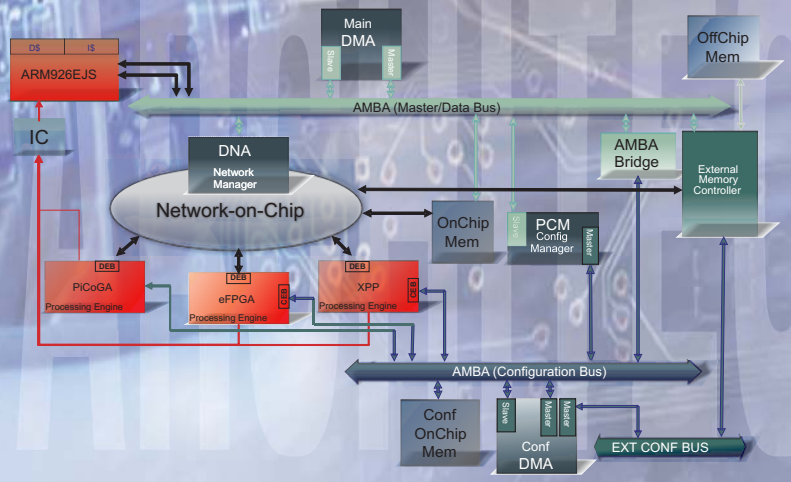
# MORPHEUS

**Multi-purpOse dynamically Reconfigurable Platform for intensive HEterogenoUs proceSsing**

**This project increases performance, flexibility and time to market of embedded systems thanks to an heterogeneous dynamically reconfigurable architecture and an associated software-like development toolflow.**

## HARDWARE

**Different to other approaches, the MORPHEUS platform architecture addresses high performance reconfigurable computing for general purpose applications. The heterogeneous reconfigurable engines (HREs) support the different flavours of reconfigurable computing, which are implemented as coarse, mid, and fine grain reconfigurable architectures. The hardware-platform consists of the following devices.**




**- General Purpose Processor (ARM926)**
Control, synchronization and housekeeping is handled by an ARM 926EJS embedded RISC processor.

**- Embedded FPGA (Abound Logic FlexEOS)**
The Abound Logic FlexEOS is a lookup table based fine grain reconfigurable device – also known as embedded Field Programmable Gate Array (eFPGA). As any FPGA, it is capable to map arbitrary logic up to a certain complexity. Provided register and memory resources are matching the specifics of the implemented logic.

**- Arces PiCoGA Array**
The PiCoGA is a medium-grained reconfigurable array consisting of 4-bit oriented ALUs and 4-bit LUTs. The architecture is mostly targeting instruction level parallelism, which can be automatically extracted from a C-subset language called Griffy-C.

**- PACT XPP Array**
The PACT XPP is a coarse grain reconfigurable array primarily targeting algorithms with huge computational demands but mostly deterministic control- and dataflow. Further enhancements based on multiple, instruction set programmable, VLIW controlled cores featuring multiple asynchronously clustered ALUs also allow efficient inherently sequential bitstream-processing.

**- Network-on-Chip**
To support a good utilization of all the three reconfigurable engines –even for general purpose– they are interconnected by a high speed NoC, which allows a close coupling of the HREs.

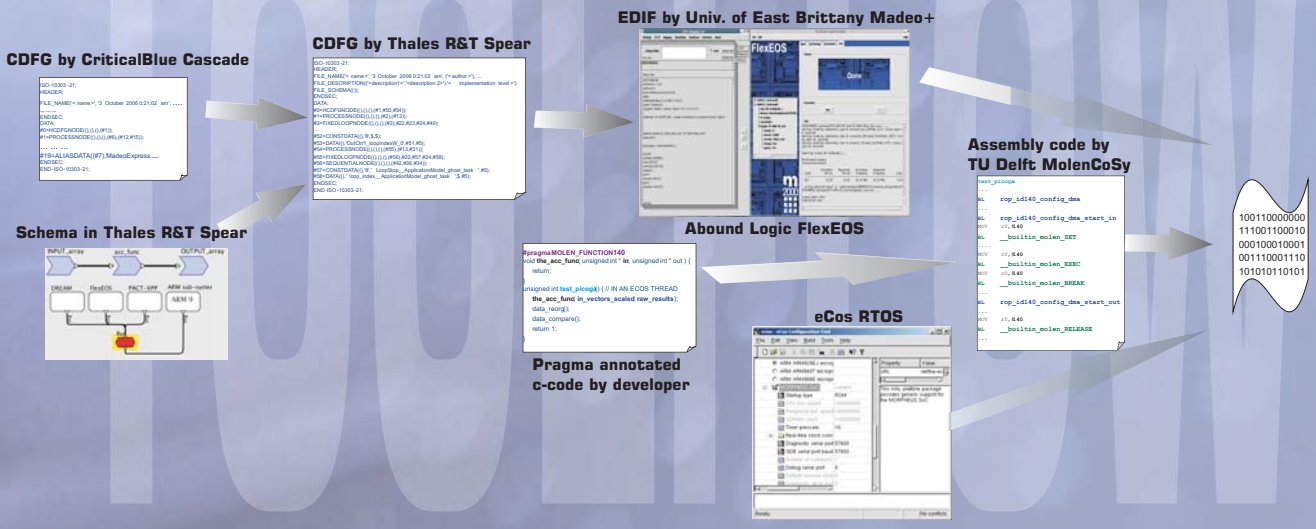
**- Hardware Services**
As dynamic reconfiguration might impose a significant performance demand for the ARM processor, a dedicated reconfiguration control unit is integrated to serve as a respective offload-engine. A network controller has also been designed featuring besides setup mechanisms for data transfers a hardware handshaking protocol to support synchronisation between communication and computation. These services reduce the workload of the main micro controller.

## SOFTWARE

**Each component has ist own development environment. The developer will be supported by combining the existing and extended tools to form an integrated toolchain.**

- Existing c-code can be used as input.
- Developer identifies kernels
- Control Data Flow Graph extracted from kernel

- Data Flow between kernels captured in schema
- Resulting CDFG implemented on reconfigurable engines
- Calls to kernel replaced by system calls




## DEMO

**The services made available by the hardware architecture as well as the techniques given by the developed tool flow can be applied whenever systems need to adapt to changing environments/requirements, especially when there are severe constraints upon cost/size/power of the computer hardware. Within this project, these scenarios are demonstrated by industrial applications from four domains.**

### Professional video
**- Film grain noise reduction**
Digital post production of HD-Video and especially digital film is one of Thomson's key business areas – both in terms of providing respective services to film studios and manufacturing therequired equipment. Thomson is also the leading manufacturer of acquisition devices (i.e. data sources) for digital post production (commonly referred to as Digital Intermediate or DI). These are either Film-Scanners scanning conventional film with resolutions of up to 4096×3112 pixels atframe rates up to 7.5 frames/s (or smaller resolutions with respectively higher frame rates) or digital cameras with HD (1920x1080) frame formats but full (4:4:4) RGB colour resolution at 10 bits per pel per colour.

### Network routing systems
**- In-service reconfiguration of SoCs**
The application to be implemented on the MORPHEUS platform is a reconfigurable network node based on the Ethernet protocol. The overall goal is to develop a system that monitors the data stream received via Ethernet and identifies configuration data on the basis of the destination address in the Ethernet header. The Optical Transport Unit (OTU) is the frame defined in ITU standard G.709 for the data transmission in optical networks. The frame consist of three parts . The overhead section, the payload section and the FEC section (forward error correction). The payload contains the data of ATM, SDH, Ethernet etc. The overhead bytes are used for quality management and to control repeaters and multiplexers in the data path. Some of these overhead bytes are reserved for special purposes i.e. they have no defined function and can be used in different ways.

### Broadband wireless access systems
**- IEEE 802.16j draft PHY**
The application targeted by ICOM is the emerging IEEE 802. 16j standard. The latest standard currently in force from the IEEE 802.16 family is 802. 16e, the basis for Mobile WiMAX technology. This standard mandates the use of Orthogonal Frequency Division Multiple Access (OFDMA) technology for the physical layer and provides all necessary support in the physical and MAC layers for mobility management, such as network entry, handover, etc. The next standard, 802.16j, currently in preparation, extends the concepts defined in . 16e by adding the possibility of multi-hop communication between mobile and base station.

### Homeland security
**- Information extraction from intelligent cameras**
The system targeted by TOSA is a general purpose (multi applications) image processing system for vision applications. The motivation to move from application dedicated architectures to general purpose reconfigurable image processing systems is the following: Traditional implementation of an image processing algorithm consists in using a FPGA and hardwiring the algorithm in VHDL onto this FPGA. Such an approach is acceptable as far as only very simple image processing algorithms are considered. The typical example is a pre-processing algorithm for use in image display systems, the goal of which being to raise the image up to a given level of quality.

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