

# Application-Specific System-Level Design Space Exploration for Heterogeneous Multiprocessor Embedded Platforms



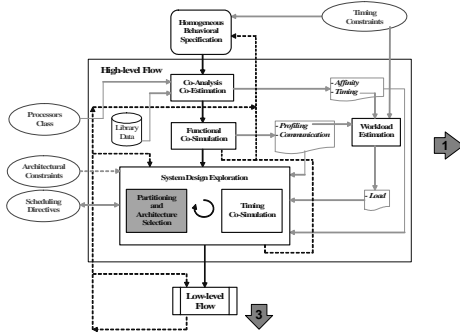
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## Overview

- This project addresses the problem of the co-design of heterogeneous multiprocessor platforms tailored to embedded applications
- In particular, the presented work starts from an existing co-design flow with the aim to propose innovative extensions to the system design exploration task
- Such extensions allow the methodology to propose an HW/SW partitioning of the specification, mapping this one onto an automatically selected heterogeneous architecture, being aware not only of the computational issues
  - i.e. automatic selection of the heterogeneous executors composing the platform
- but also to take into consideration the communication ones
  - i.e. automatic selection of the links and the topology interconnecting the selected executors

Follow the navigation tips!

## The System-Level Co-Design Flow



## The System-Level Co-Design Flow

- The entry point is a behavioral description of the application
- The first step (*Co-Analysis&Co-Estimation*) extracts some important data about the system
  - The *affinity* of each functionality toward the considered processing elements and a set of estimations of the time required for the execution of each single operation
- Then, the specifications are simulated to verify correctness with respect to typical input data sets, extracting data characterizing the dynamic behavior of the system
  - Profiling and Communication Bandwidth*
- Combining the data provided by the first step with the *timing constraints* allows the estimation of the *load* associated with each functionality
  - The analysis of such data is useful to evaluate the number of processors and the level of load balancing
- Two iterative steps constitute the *System Design Exploration* task
  - Partitioning and Architecture Selection*, and *Timing Co-Simulation*

## Architectural Elements & Metrics

### Possible Links

- Point-to-Point
- Bus
- Mesh

### Characterization

- Max Bandwidth
- Max #Executors
- Cost (€)

### Saturation Index

$$I_s = 1 - \sum_{j=1}^m \frac{a_j \cdot b_j}{m}$$

### Exploitation Index

$$I_e = 1 - \sum_{j=1}^m \frac{a_j}{m}$$

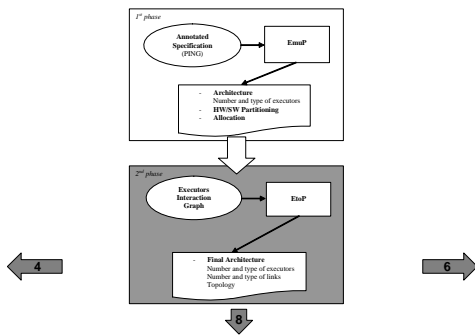
### Total Cost

$$I_c = \sum_{j=1}^m \frac{c_j}{m \cdot c_{max}}$$

### Cost Function

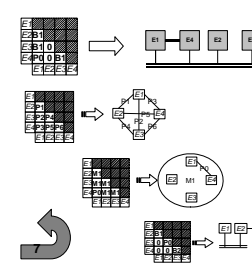
$$CF = w_s \cdot I_s + w_e \cdot I_e + w_c \cdot I_c$$

## Partitioning & Architecture Selection Step

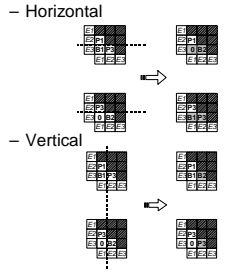


## Individuals & Cross-Over

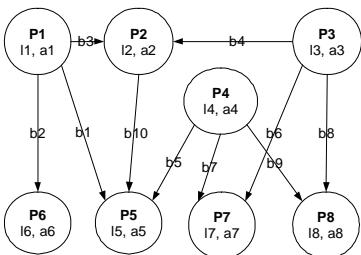
### Possible Individuals



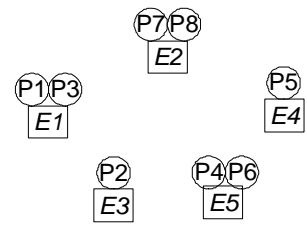
### Cross Over



## Example: Step 1 Annotated Specification (CSP)



## Example: Step 2 Executors/Allocation View



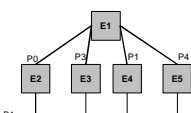
## Example: Step 4 Results

- EIG
  - BW1=250
  - BW2=200
  - BW3=200
  - BW4=150
  - BW5=250
  - BW6=50
  - BW7=50
- Links Characterization
  - max bandwidth, max number of executors, relative cost):
    - PTP=(500, 2, 1)
    - BUS=(250, 8, 2)
    - MESH=(200, 80, 5)
- CF weights
  - WB=WE=0.35
  - WC=0.3

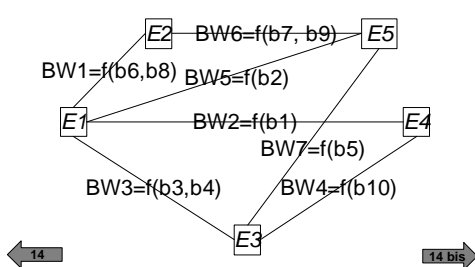
### Best Individual

- CF=0.225
  - IB=0.44
  - IE=0.1
  - IC=0.12

E1	P1	P2	P3	P4
E2	P1	P2	P3	P4
E3	P1	P2	P3	P4
E4	P1	P2	P3	P4
E5	P1	P2	P3	P4
E6	P1	P2	P3	P4
E7	P1	P2	P3	P4
E8	P1	P2	P3	P4



## Example: Step 3 Executors Interaction Graph



## Example: Step 4 bis Results

- EIG
  - BW1=250
  - BW2=200
  - BW3=200
  - BW4=150
  - BW5=250
  - BW6=50
  - BW7=50
- Links Characterization
  - max bandwidth, max number of executors, relative cost):
    - PTP=(500, 2, 4)
    - BUS=(250, 8, 2)
    - MESH=(200, 80, 5)
- CF weights
  - WB=WE=0.35
  - WC=0.3

### Best Individual

- CF=0.285
  - IB=0.34
  - IE=0.2
  - IC=0.32

E1	P1	P2	P3	P4
E2	P1	P2	P3	P4
E3	P1	P2	P3	P4
E4	P1	P2	P3	P4
E5	P1	P2	P3	P4
E6	P1	P2	P3	P4
E7	P1	P2	P3	P4
E8	P1	P2	P3	P4

