Design Tools Session

Multi-granularity NoC simulation framework for early phase exploration of SDR platforms[*]

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Abstract

After the introduction of the first multi-core processor chip in 2001 multiprocessing has developed dramatically. Today, nearly all processor chips use multiple cores in an attempt to deliver more system performance within their power-constrained environment. The related trend at the embedded system design industry is the appearance of an increasing number of hardware components on a single chip pressured by rising performance requirements of embedded applications and manufacturing cost. The combination of this trend and the power consumption issues led to the rise of the MPSoC paradigm which demonstrates significant advantages over more traditional designs with the respective reflection at the complexity of the design process of hardware and software. Moreover, it is widely acknowledged that early design decisions have the most significant impact on the final system performance and power consumption. Furthermore, new applications such as Software Defined Radio (SDR) make usage of the additional resources offered by these MPSoC platforms. SDR terminals are critical to enable concrete and consecutive inter-working between 4th generation wireless access systems or communication modes. The next generation of SDR terminals is intended to have heavy hardware resource requirements and switching between them will introduce dynamism in respect with timing and size of resource requests. The traditional approach to design and development SDR and Cognitive Radio SDR platforms is based on the worst-case scenario of the dynamic software requirements in order to determine the hardware resources characteristics. The SDR system can dynamically adopt appropriate modes to get the optimal quality of the communication service. The increased demands on performance combined with an increase in user control and interactivity with the environment have a significant impact on the resource requests. The latter is becoming more dynamic because different wireless protocols must be switched at unknown timing moments. On the other hand, it has been proved that run-time resource management optimizations can reduce resource requests without affecting significantly the QoS and the interaction between user and application. The key for the software developers who design dynamic wireless applications is to incorporate such run-time mechanisms without over-provisioning the resources.

The real challenge is to estimate the performance characteristics of the software including the impact of run time mechanisms, at a time when no source code exists. Thus, it is clear that in a design process of a dynamic application a hardware-software co-design simulation framework should be available, capable of dealing with a combination of hardware, software and run-time models in order to take into account the various dependencies between hardware and software development and their refinement efforts. Especially it should be possible to create this in a very early phase of the development process. This work presents a system-level framework/tool combined with a cycle-accurate NoC simulation environment that enables the simulation of such complex, dynamic hardware/software SDR designs. The platform specifications are represented as a virtual architecture by a coarse-grain simulator described in SystemC that includes a set of configuration parameters. The key of our approach is that our simulator environment provides automatic wrapper tools able to explore the SDR platform architecture/parameters and simultaneously transmit the interconnection traffic in a cycle-accurate NoC simulator giving the opportunity to examine the impact of different topologies at the system bandwidth at execution time. Thus, we can do an exploration, which can pinpoint at a very early design phase the platform component requirements for future SDR applications. This approach shows a drastic design-time reduction with cycle-accurate simulation accuracy.